Spacecraft Uplink, Downlink, and Intercomm unications in a Space-Qualified ASIC Chip Set

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ABSTRACT

This paper' describes the functionality of four application specific integrated circuits (ASICs) developed for the Cassini spacecraft. The four ASICs are used on the spacecraft in the Command and Data Subsystem to receive uplink data, transmit downlink data, and provide intercommunications within the spacecraft via a 1553B bus. Implemented in the ASICs is a portion of the spacecraft uplink and downlink protocol specified in the Consultative Committee for Space Data Systems (CCSDS) standard. The CCSDS standard is a widely used, international standard. The ASICs also provide additional functions often required in a Command and Data Subsystem such as a spacecraft clock, a "fault detection unit", and DMA, The ASICs, produced in Honeywell's RICMOS technology, are radiation hard, single event upset hard, and highly reliable (Class S). The implementation in space-qualified ASICs of uplink, downlink, and spacecraft intercommunication functions which meet widely used standards is expected to have applications in a variety of spacecraft.

INTRODUCTION

The Command and Data Subsystem on the Cassini spacecraft performs uplink, downlink, and spacecraft intercommunications functions. The Cassini spacecraft, currently under development at the Jet Propulsion Laboratory, will be launched in 1997 on a 12 year mission to Saturn, A block diagram of the Command and Data Subsystem is shown in Figure 1. The primary hardware components in the subsystem are a 1750A computer and four ASICs.

The Hardware Command Decode (HCD) ASIC is used to receive and decode uplink commands. Implemented in the ASIC is the "receiving end coding layer" of the CCSDS Telecommand standard. The TDL ASIC supports the CCSDS Telemetry Transfer Frame protocol. It performs Reed-Solomon encoding on the telemetry data and formats it into a downlink Transfer Frame. It also contains a Spacecraft Clock. The SSRIU ASIC provides software with an interface to a Solid State Recorder. It also provides software with a data interface to the RSDL. The XBA ASIC works in conjunction with the UTMC

BCRTM chip to act either as a 1553B RT or BC. The XBA ASIC provides software with a simple interface to the 155311 bus. All of the ASICs communicate with the host computer via the ISB bus, which is a 16-bit, parallel, fully-interlocked, asynchronous, mu]ti-master bus.

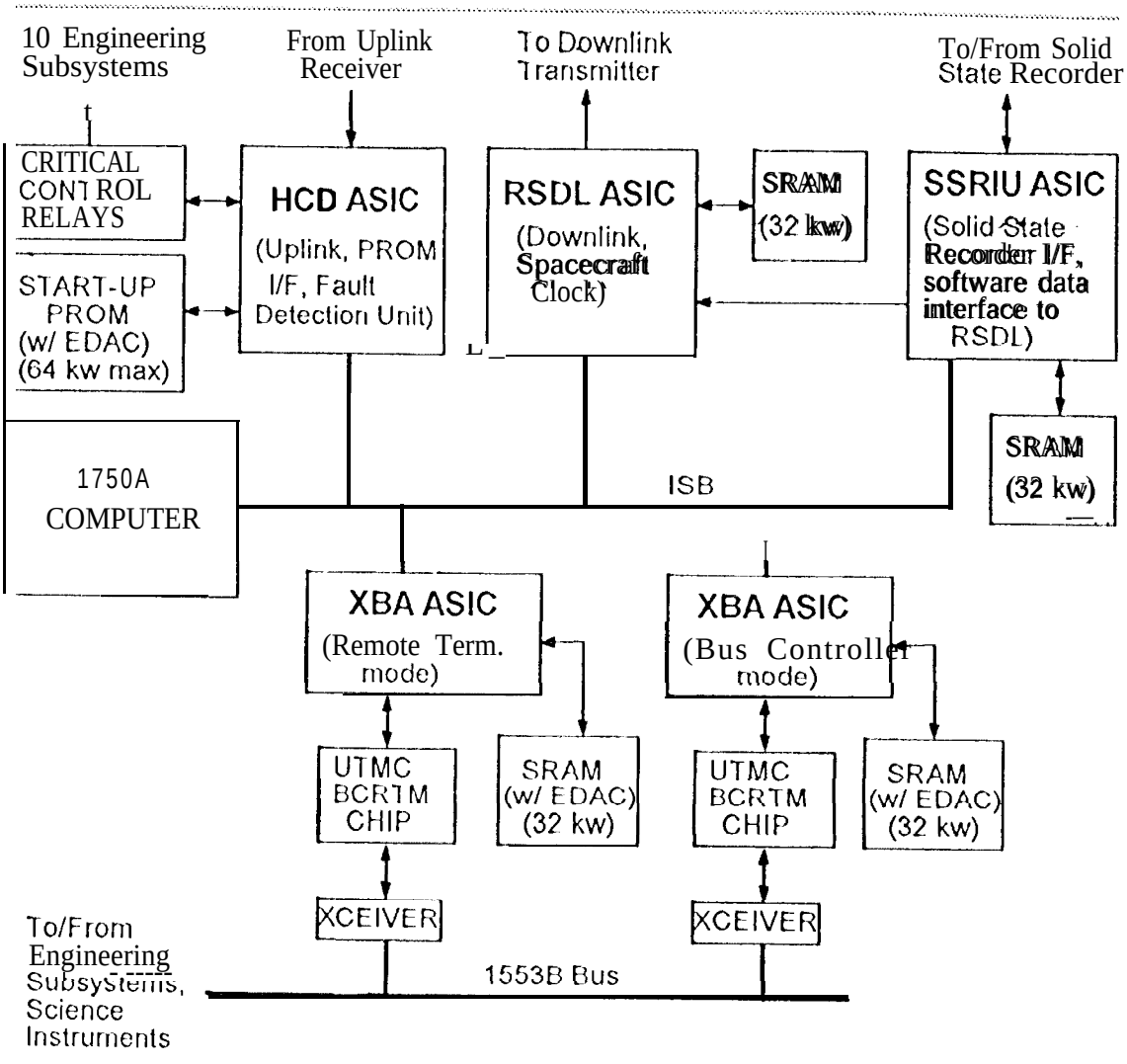

Figure 1: Cassini Command and Data Subsystem Block Diagram

Body

The following topics are addressed in the body of this paper:

(1) HCD ASIC Functional Description

(2) RSDL ASIC Functions] Description

(3) SSRIU ASIC Functional Description
(4) XBA ASIC Functional Description
(5) Inter-Subassembly Bus (ISB) Functional Description
(6) Implementation Description
(7) Development Status

(1) HCD ASIC Functional Description

Overview: The Hardware Command Decode (HCD) ASIC is used to receive and decode uplink data. Implemented in the ASIC is the "receiving end-coding layer" of the CCSDS Telecommand standard. The ASIC receives a serial, digital data stream of uplink data from the antenna receiver electronics. The ASIC will preform one of two types of error detection/ correction on the uplink data: single bit error correction and double bit error detection; 01 triple bit error detection (no correction). The ASIC also supports direct ground control of up to 32 relays and *24* discrete outputs via Virtual Channel O commands. These relays and discrete outputs allow ground control of critical functions independent of the flight software. The ASIC also contains a "fault detection unit" which provides a watchdog timer, interrupt control support, reset control, and eight discrete outputs which support the exchange of system "health" and other information between redundant systems.

Each of the following three functions will be discussed below:
(A) Uplink Data Decoding
(B) Critical Enables
(C) Fault Detection Features

(A) Uplink Data Decoding: The primary function performed by the HCD ASIC is to decode the uplink data stream, which is formatted in accordance with the CCSDS Telecommand standard. The ASIC receives a serial, digital, NRZ-L data stream, as well as a clock and a Lock signal from the uplink data receiver. The format of the data stream is illustrated in Figure 2. As can be seen in Figure 2, the data stream has four levels of formatting, At the top level, the uplink data stream is composed of three data structures, which are described below.

Acquisition Sequence: The Acquisition Sequence is an alternating pattern of ones and zeros, starting with either one or zero. It is used at the start of an uplink session to allow the uplink receiver to "lock" onto the data stream. The HCD ASIC requires that this pattern be a minimum of two bytes in length.

-Command Link Transmission Unit (CLTU): The CLTU contains the actual data being sent to the spacecraft. The format of the CLTU is discussed below.

Idle Sequence: The Idle Sequence is an alternating pattern of ones and zeros. It allows the uplink receiver to maintain lock in the absence of CLTUs.

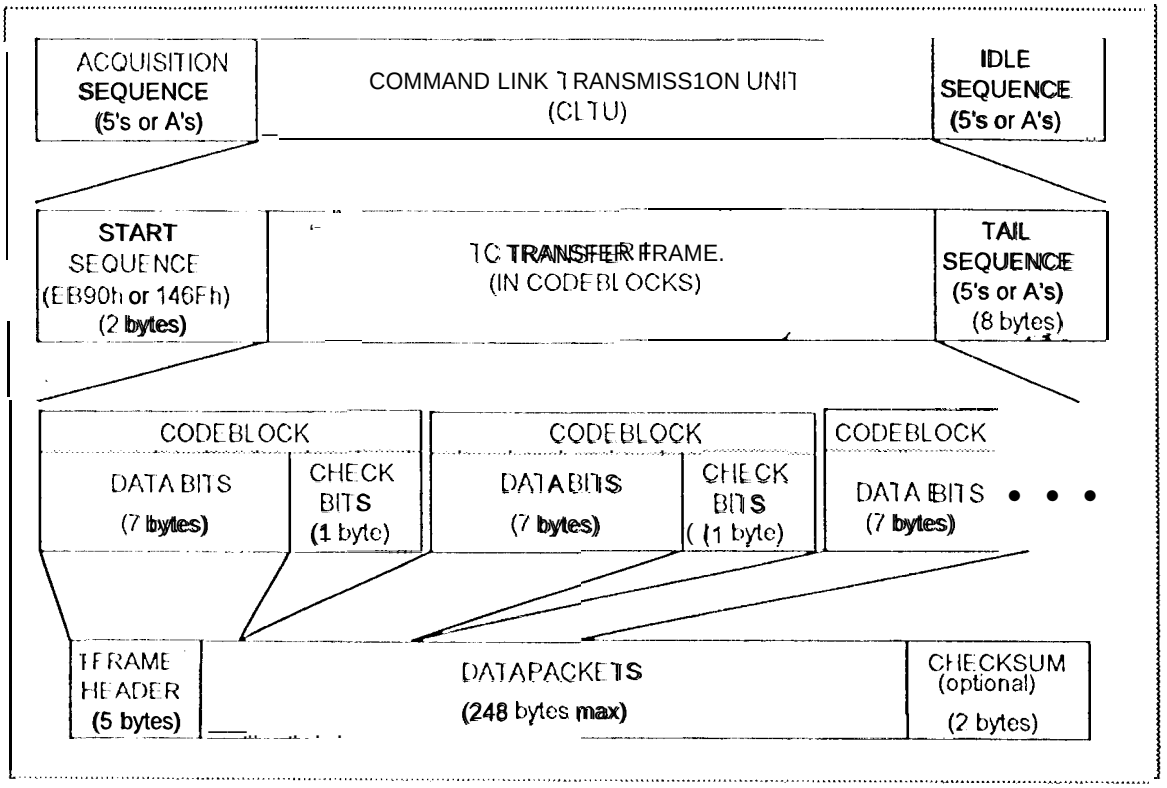

Figure 2: Uplink Data Format

A CLTU is composed of three fields, as shown in Figure 2. Each field is described below.

Start Sequence: The Start Sequence consists of 16 bits and has the value EB90 hex if the data polarity is positive, and 146F hex if the data polarity is negative. The ASIC uses the Start Sequence to identify the beginning of a CLTU. It also uses the Start Sequence to determine the polarity of the data.

TeleCommand Transfer Frame(s): The CLTU may contain several TeleCommand (TC) Transfer Frames. Each TC Transfer Frame consists of several TC Codeblocks. Each TC Codeblock consists of 56 information bits, 7 check bits and 1 fill bit, as shown in Figure 2. The check bits are generated using a (63,56) modified Bose-Chaudhuri-Hocquenghem (BCH) code. This code is specified in the CCSDS TeleCommand standard.

Tail Sequence: The Tail Sequence consists of 64 bits and has the value S555 S5S5 5555 55ss (hex) if the data polarity is positive, and AAAA AAAA AAAA AAAA (hex) if the data polarity is negative. The Tail Sequence is used by the ASIC to identify the end of a CLTU.

At the. lowest level of data encoding, the Data fields from each Codeblock are pieced together to form a Frame Header, Frame Data Field, and an optional Checksum, as shown in Figure 2. As will be discussed later, the. ASIC presents Codeblocks to the software. The flight software pieces Codeblocks together to form the Frame Header, Data Field, and Checksum. The Frame Header format is shown in Figure 3.

VERSION NUMBER	BYPASS FLAG	CONTROL COMMAND FLAG	SPARE	SPACE CRAFT ID	VIRTUAL CHANNEL ID	SPARE	FRAME LENGTH	FRAME SEQ NUMBER
(2 bits)	(1 bit)	(1 bit)	(2 bits)	(10 bits)	(6 bits)	(2 bits)	(8 bits)	(8 bits)

Figure 3: Frame Header Format

The ASIC decodes this complex data structure, performs error detection and correction, and places the data field from each Codeblock into a software buffer, as is described below.

Data Decoding Operation: The state diagram in Figure 4 illustrates the data decoding operation of the ASIC. The HCD ASIC receives a LOCK signal from the spacecraft uplink receiver. When the LOCK signal is asserted, it indicates that the input data to the ASIC is valid data. When the LOCK signal is deasserted, it indicates that the data is not valid and so the ASIC ignores the data,

The uplink data decode function in the HCD ASIC operates as follows. Whenever the LOCK signal is deasserted, the ASIC transitions to the Inactive State and ignores the uplink data stream. Once the LOCK signal is asserted, the ASIC transitions to the Search State and starts searching to uplink data stream for the Start Sequence. Once the Start Sequence is detected, the ASIC transitions to the Decode State and starts decoding Codeblocks. When a Codeblock is received, error detection and correction is performed and then Codeblock is placed in a data buffer that can be accessed by software. When a Codeblock with an uncorrectable error is decoded, the ASIC transitions back to the Search State and starts searching for the Start Sequence. The Tail Sequence at the end of a CLTU, as shown in Figure 2, contains an uncorrectable error. Therefore, when a Tail Sequence is received, it forces the ASIC back to the search state.

It should be noted that except for Virtual Channel O commands (which are discussed in the next section), the format and contents of the data in each Codeblock is a "don't care" to the ASIC. Software must fetch the Codeblock from the data buffers and perform the necessary format checks and data interpretation.

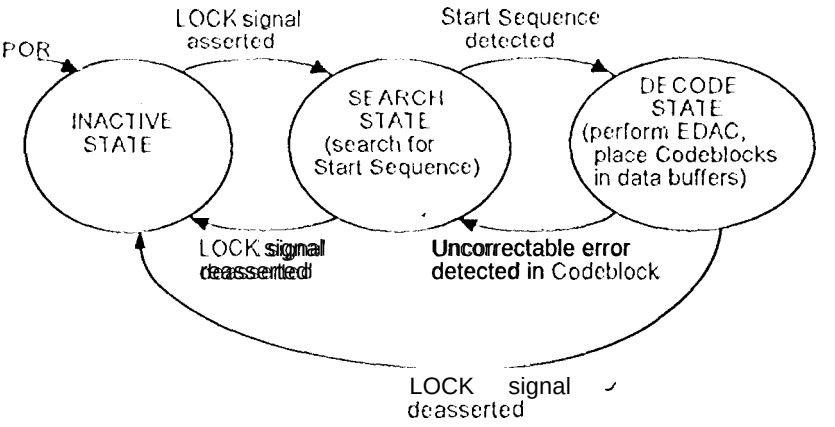

Figure 4: Data Decoding

Error Detection and Correction: As described earlier, each Codeblock contains seven parity check bits, which allow error detection and correction to be performed on the Codeblock. The ASIC has two modes of error handling, which is user selectable. in one mode, single errors arc corrected, and double bit errors arc detected. In the other mode, single, double, and triple bit errors arc detected, but there is no correction. If the uplink channel is very noisy, the user may want to have triple bit error detection. If the uplink channel is not very noisy, the user may prefer to have single bit error correction,

Software Interface: The HCD ASIC contains two data buffers which arc used to pass the uplink data to the software. Each data buffer consists of four 16 bit registers. Thus, each data buffer can hold one 64 bit Codeblock. At any point in time, one buffer is the active buffer that the ASIC is writing data into, while software is reacting data from the other buffer. The ASIC also contains a status register which allows software to determine which buffers arc full, if the buffers have been overrun, if the receiver is in lock, if any err ors have been detected in the data, ancl other status. The ASIC can also be programmed to interrupt the host processor whenever it fills a buffer.

(B) Critical Enables: The HCD ASIC allows the ground to directly control up to 32 non-volatile relays and 24 volatile discrete outputs via Virtual Channel O Transfer Frames. These relays and discrete outputs, referred to as Critical Enables, allow the ground to control critical functions independent of flight software.

The virtual channel number is specified in the Transfer Frame Header, as shown in Figure 3. The Virtual Channel 11) bits are used to logically multiplex a single physical telecommand da(a channel into 64 logical channels. The ASIC imposes two restrictions on the use of these channels:

(1) Virtual Channel O is reserved for "hardware commands", which toggle the Critical Enables.

(2) When using Virtual Channel O, the CLTU may contain only one Transfer Frame.

once the ASIC detects a Start Scquc.net, it then checks the Virtual Channel ID bits in the Frame 1 leader in the first TC Transfer Frame. When a Virtual Channel O Transfer Frame is detected, the ASIC checks that the Spacecraft ID bits and some of the other bits in the Frame 1 leader are correct. If they are correct, the ASIC then writes to the Critical Enables specified in the Frame Data Field, ant{ places the Codeblock in the software data buffer. When a non-Virtual Channel O Transfer Frame is detected, the ASIC simply places the. Codeblock in the software data buffer without checking any of the other bits in the Frame 1 leader.

(C) Fault Detection Functions: The 1 ICD ASIC provides a variety of fault detection-related functions independent of uplink that are often needed in spacecraft data systems. All of these functions operate independently, and the user has the option of either using or disabling each function. Each function is briefly described below,

(1) A '[sophisticated" watchdog timer: Software must write three specific data words to three specific, non-contiguous addresses within a fixed amount of time (i.e. an RTI period), or a system reset will be issued.

(2) Interrupt control support: The ASIC has eight input pins that can be connected to generic interrupt sources by the user.

(3) Reset control: The reset contr o] function allows up to six different reset sources, three of them user definable, to produce a reset of the host subsystem.

(4) Eight discrete inputs and eight discrete outputs which support the exchange of system "health" and other information between redundant systems.

(5) Start-up PROM interface: The ASIC also provides a software interface to start-up PROM. The interface supports up 64 kwords (16 bit words) of PROM. The ASIC also provides single bit error correction, double bit error detection on the PROM data.

(2) *RSDL ASIC Functional Description*

The R SDL ASIC contains two distinct functional blocks: Reed-Solomon encoder, and a Spacecraft Clock. Each function is described below.

(A) Reed-Solomon Encoding: The RSDL ASIC, in conjunction with the SSRIU ASIC and Flight Software, forms Telemetry Transfer Frames as per the CCSDS standard, The Telemetry Transfer Frame format is shown in Figure 5. 1 Each of the Transfer Frame fields arc described below.

Sync Marker: The Sync Marker consists of 32 bits and has the value 1 ACF FC1D hex. It is used on the ground to determine the start of a Transfer Frame.

1 leader and Data Field: The engineering and science data that needs to be sent to the ground is found in this field. The formatting of this data with Source Packet Headers, Transfer Frame Headers, etc. as per the CCSDS standard is performed by software. The RSDL ASIC does not require that the data format met the CCSDS standard.

Reed-%lmnon Check Bits: These check bits allow error detection and correction to be performed on the ground on the Transfer Frame Header and Data field.

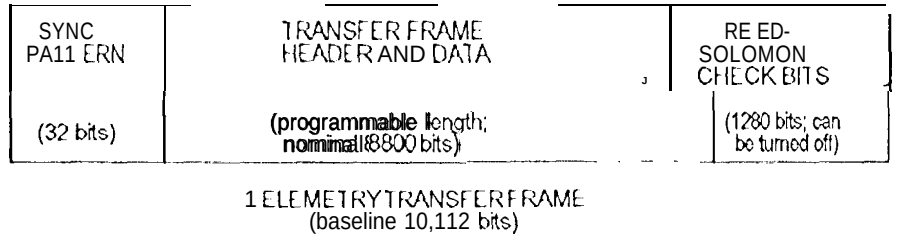

Figure 5: Telemetry Transfer Frame Format

A Transfer Frame is formed by the 1< SDL ASIC as follows:

(1) Flight software forms the} leader and Data field for several Transfer Frames

(2) Flight software then loads the Header and Data fields into one of the two Downlink (DL) Buffers in the SSRIU ASIC. Software loads the DL Buffers via the ISB. The SSRIU DL Buffers behave as ping-pong buffers. At any point in time, Transfer Frame 1 leader and Data fields arc being read from the active DL Buffer by the 1< SDL, while software is loading the inactive buffer with data. This is illustrated in Figure 6. A DL Buffer can hold anywhere from one to eight Transfer Frame Data and I leader fields.

(3) On the Cassini spacecraft, the DL Buffers can also be loaded with recorded 1 leader and Data fields from the Solid State Recorder. This is done via a serial port and is orchestrated by flight software. The use of the serial porl is optional,

(4) The 1< SDL ASIC autonomously reads data from the active SSRIU DL Buffer. This is done through a dedicated interface between the SSRIU and 1{ DL ASICs. When the RS DL reaches the. end of the active DL Buffer, it switches to the other buffer.

(5) After a buffer swap, the RS DL ASIC first sends the Sync Marker for the next Transfer Frame to the RF transmitter electronics.

(6) Next, the RSDL ASIC reads the I leader and Data field for the next Transfer Frame from the active DL Buffer and sends it to the RF transmitter electronics.

(-/) As the RSDL ASIC reads the 1 leader and Data field from the active DL Buffer, it calculates the Reed-Solonlon check bits for the Transfer Frame. After sending the Header and Data field to the RF transmitter electronics, it sends the Reed-Solomon check bits.

(8) Steps (5) to (7) are repeated until the end of the active DL Buffer is reached and another buffer swap **occur-s**

The size of the Transfer Frame being sent to the RF transmitter electronics is programmable. The size of the DL Buffers and their location in SSRIU RAh4 arc also programmable. Software also has the option of turning Reed-Solomon encoding off.

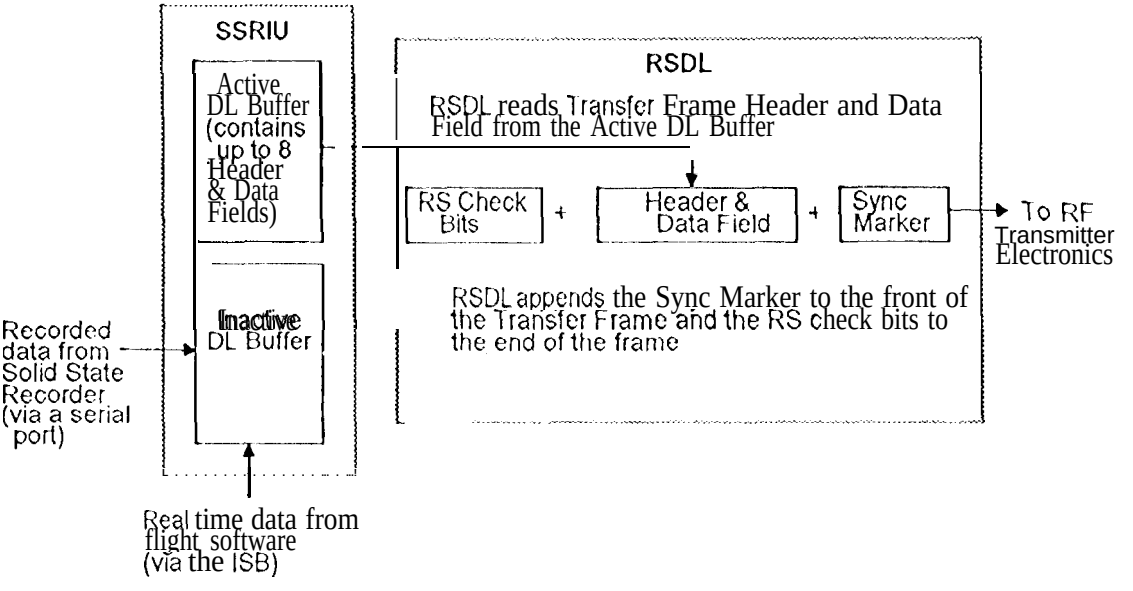

Figure 6: Formation of Transfer Frames by the RSDL ASIC

The 1< S1)1. ASIC supports 127 different downlink data rates ranging from *5* to *248,850* bits per second. The downlink data rate is programmable by software.

The ASIC sends digital, NRZ-L, serial data to the RF Transmitter electronics. It also sends a clock with a frequency of' six times the data rate. This interface cannot be turned off; whenever the RSDL ASIC is powered, it constantly sends Transfer Frames to the RF Transmitter electronics.

(B) Spacecraft Clock: On the Cassini spacecraft, the Spacecraft Clock is used to trigger the execution of time-based commands and sequences, Main engine burns, pyro firings, science collection, etc. is all triggered by the Spacecraft Clock. The Spacecraft

Clock consists of a 46 bit counter which keeps track of elapsed time with a range of O to 4,294,967,295.999 seconds (~136 years). It has a resolution of 61.031 microseconds. Flight software can load the Spacecraft Clock with a new value, provided the load function is enabled by the ground. Provisions have been made to allow the Spacecraft Clock in the two redundant Command and Data Subsystem strings to be easily and precisely kept in synchronization. An 8 Hz Real Time Interrupt (RTI) signal derived from the Spacecraft Clock is used as the basis for scheduling software tasks.

The RTI Drift Counter in the XBA ASIC allows software to detect drifts in the Spacecraft Clock. The RSDL ASIC also has a feature which allows the ground to detect drift in the Spacecraft Clock. If Spacecraft Clock drift is allowed to go undetected, sequences will get executed at the wrong time.

(3) SSRIU ASIC Functional Description

A block diagram of the Solid State Recorder Interface Unit (SSRIU) ASIC is shown in Figure 7. The SSRIU ASIC performs two primary functions, as described below.

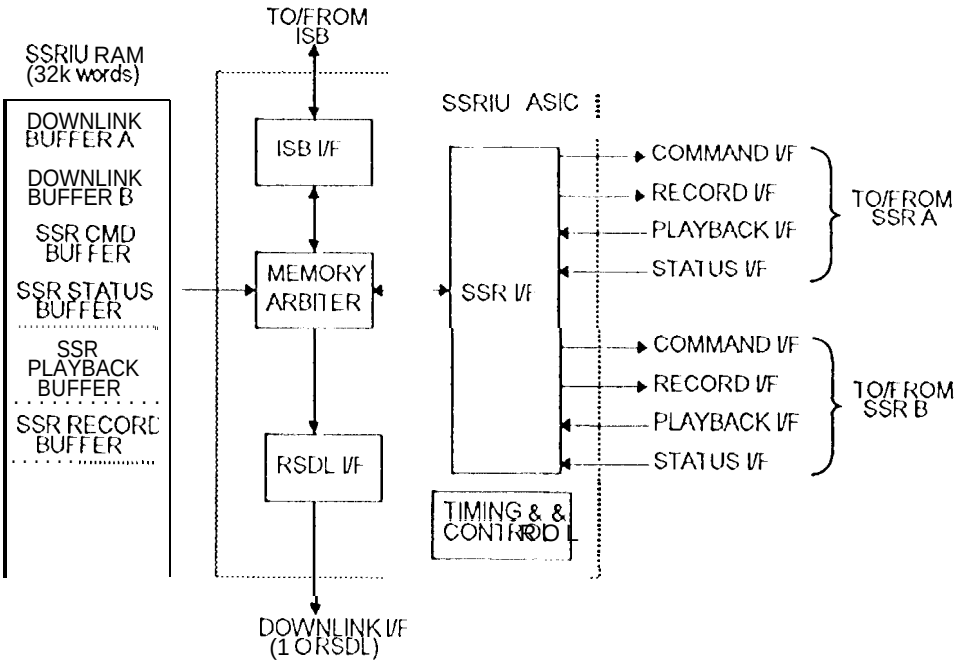

Figure 7: SSRIU ASIC Block Diagram

(A) Solid State Recorder Interface: The SSRIU ASIC provides software with an interface to the TRW Solid State Recorder (SSR) that is used on the Cassini spacecraft. This interface consists of four digital, synchronous, serial ports:

(1) Command Interface: This port is used to send commands to the SSR.
(2) Record Interface: This port is used to record data cm the SSR.
(3) Playback Interface: This port is used to playback data from the SSR.
(4) Status Interface: This per-[is used to read SSR status.

Each of the four ports consist of four signals: Data, Clock, Enable, and Ready. Each port operates at 1.5M bits per second. The four ports operate independently and may operate simultaneously. The Clock signal is always sourced by the SSRIU ASIC. The SSRIU ASIC initiates a transaction by asserting the Enable signal. The SSR responds with the assertion of the Ready signal. The transaction starts with the assertion of the Ready signal.

(B) RSDL Data Interface: The SSRIU ASIC provides software with a data interface to the RSDL ASIC. This function was described in description of the RSDL ASIC.

(4) *XBA ASIC Functional Description*

The Cross-string Bus Adapter (XBA) ASIC performs two primary functions:
(1) The ASIC, along with the UTMC BCRTM chip, can function as a Remote Terminal (RT) on a 1 553B Bus when the ASIC is operating in RT mode.
(2) The ASIC, along with the BCRTM chip, can function as a Bus Controller (BC) on a 1553B Bus when the ASIC is operating in BC mode.

The Military Standard 1553B bus is serial, transformer-coupled, Manchester encoded, redundant, and operates at 1M bit per second. The devices on the bus consist of a single BC, which controls all bus traffic; and multiple 1<'1's, which act as bus slaves.

A block diagram of an RT or BC using the XBA ASIC can found in Figure 8. As can be seen in the block diagram, an R']' or BC consists of an XBA ASIC, BCRTM chip, 32 kwords of RAM, and a 1553 interface, RT and BC hardware is identical except for the operating mode of the XBA ASIC. Each Command and Dat a Subsystem on Cassini cent sins an RT and a BC to allow communicat ion between the redundant strings, Only the BC in the "Prime" Command and Data Subsystem is allowed to function, the BC in the "Backup" string is disabled until the string becomes "Prime".

The 1553B protocol is implemented in the UTMC BCRTM chip. The XBA ASIC provides software with an interface to the BCRTM registers and 32 kwords of buffer RAM. It also provides single bit error correction, double bit error detection on the RAM. In addition, the ASIC provides a DMA capability which allows the direct transfer of data between the 1553B bus and the host computer memory without software intervention. The ASIC also contains a watchdog timer, memory error detection and correction, and other features.

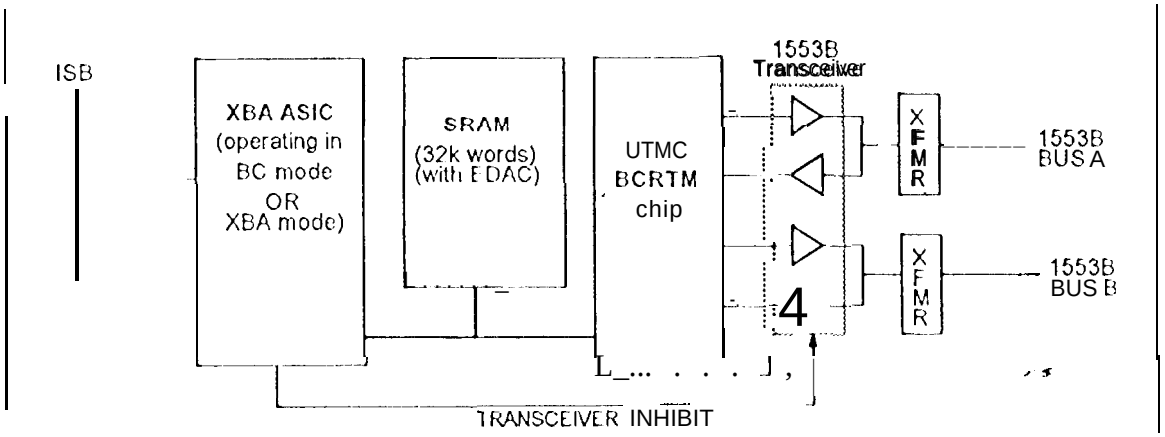

Figure 8: RT/BC Block Diagram

An overview of the functions performed by the XBA ASIC in BC mode and RT mode are presented below.

(A) BC Mode : in BC mode, one of the primary functions of the ASIC is to support the bus traffic protocol shown in Figure 9. This protocol is as described below:

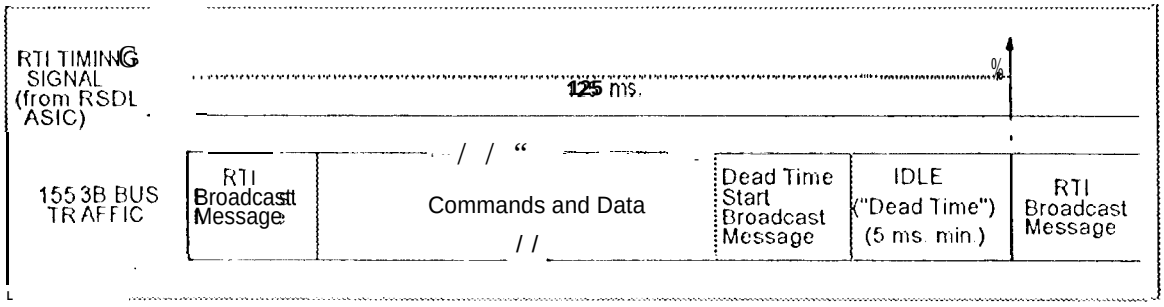

Figure 9: 1553B Bus Traffic Protocol on the Cassini Spacecraft

(1) RTI *is* an *81* Iz hardware timing signal derived from the Spacecraft (lock that is used by software to schedule tasks. It is also distributed throughout the spacecraft to allow subsystems and instruments to perform task synchronously. The ASIC uses the occurrence of RTI to trigger the start of BC transmissions on the 1553B bus. Immediately after the 1{'1'1, the BC broadcasts the 1553B "Synchronize" mode code to indicate to the rest of the spacecraft that an RTI has occurred.

(2) The BC then transmits commands and receives data over the bus as necessary.

(3) When the BC has completed its bus transactions for the RTI period, it transmits a "Dead Time Start" mode code. This indicates to user-s that there will be no

more traffic on the bus until the next 1< '1 '1. The "Dead Time" allows users to reconfigure their RT, load buffers with data for the next RTI period, etc. During ground test, the "Dead Time" can be used by ground support equipment to perform DMA peeks and pokes into the Command and Data Subsystem ISB address space. The "Dead Time" is guaranteed by the ASIC to be a minimum of 5 milliseconds in duration,

The XBA ASIC makes it easy for- software to support this bus traffic protocol, as shown in Figur c 10 below. During an RTI period, while the BCRTM chip is autonomously transmitting and receiving data from the active RAM buffer, software can be loading the inactive buffer with data for the next RTI period. Software also loads BCRTM configuration data to be used during the next RTI period into the XBA ASIC at this time. When the next RTI occurs, the XBA ASIC autonomously loads the BCRTM Control registers with the software specified configuration data. The BCRTM chip then immediately begins 155311 bus activities, starling with transmission of the "Synchronize" mode code. One of the main advantages of this design is that it eliminates 'software jitter' in the transmission of the "Synchi onize" mode code to the rest of the spacecraft.

The BC can also be programmed by software to DMA data directly to and from the host computer RAh4 instead of the BC buffer RAM. The BC does so by becoming a master on the 1 SB. The usc of this feature will conserve host computer throughput.

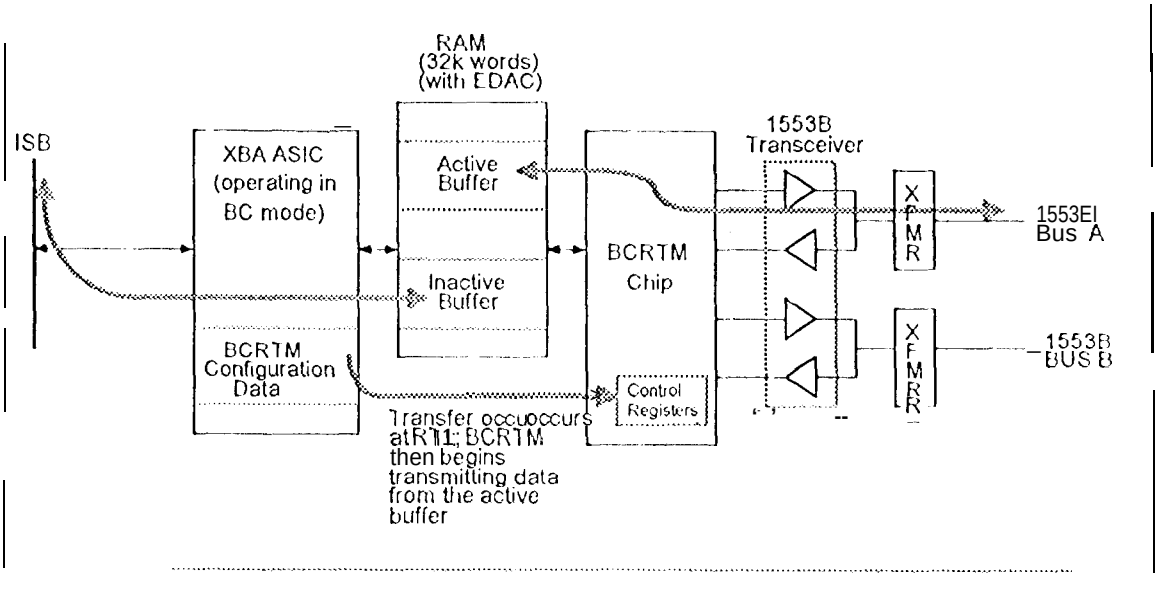

Figure 10: BC Operation

(B) RT Mode: When operating in RT mode, the primary function of the ASIC is to let software access BCRTM registers and the buffer RAM. Some additional functions performed by the ASIC are:

(1) Discrete inputs and Outputs: The ASIC has eight discrete outputs which can be set via the 1 553B bus. The ASIC also has eight discrete status inputs which can be read via the 1553B bus.

(2) Watch Dog Timer: The Watch Dog Timer is used to verify that the. RT is periodically receiving messages on the 1553B bus. It consists of a 4 second timer that is reset upon receipt of a particular 155311 message. The intent is for the BC to broadcast a Watch Dog Timer reset message every RTI period to all Remote Terminals on the bus. If four seconds elapse without the BC transmitting Ibis message, expiration of the Watch Dog Timer occurs. When the Watch Dog Timer expires, transmission on the 1553B bus by the RT is inhibited (until cleared by the BC), and the BCRTM chip is reset and initialized. This feature prevents an RT from "babbling" on both 1553B redundant buses and essentially taking down the spacecraft.

(3) RTI Drift Counter: The RTI Drift Counter allows software to detect drift in the Spacecraft Clock. It does this by measuring the time between RTIs. The XBA ASIC and 1< DL ASIC must operate off of different oscillators in order for this feature to work. Without this feature, software would not be able to detect drift in the Space.craft Clock. Of particular concern would be excessive drift due to a hardware failure, The Spacecraft Clock is used on the Cassini Spacecraft to trigger main engine burns, pyro firings, science sequences, etc. If not detected, drift in the Spacecraft Clock can result in commands and sequences being executed at the wrong time. The 1< DL ASIC also contains a feature which allows the ground to detect Spacecraft Clock drift.

(4) DMA: During ground test, the Support Equipment can become Bus Controller on the 1 553B Bus, and then use the RT to load and readout host computer memory, and to peck and poke in ISB address space in support of debugging and special tests. This capability is referred to as DMA. The XBA ASIC performs DMA by becoming a master on the ISB.

(5) Inter-Subassembly Bus (ISB) Functional Description

All four ASICs communicate to the host processor via the 1S11 bus. The. ISB is a custom bus developed at the Jet I'repulsion Laboratory. The ISB is a 16-bit, parallel, fully-interlocked, asynchronous, multi-master bus. The R SDL, SSRIU, and HCD ASICs act only as slaves on the bus. The XBA ASIC may act as a master or slave. The bus protocol is shown in Figures 11 and 12 below,

A space-qualified field programmable gate array (FPGA) is currently under development at JPL for the Mars Pathfinder spacecraft which will allow the ASIC to interface to a VME bus. The FPGA acts as a translator between the ISB and VME buses.

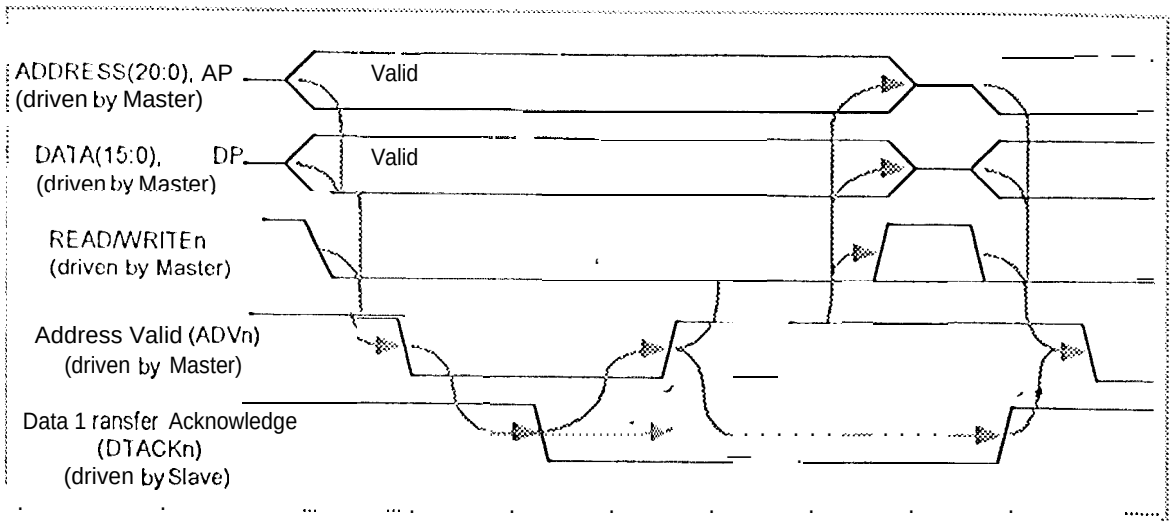

Figure 11: ISB Write Cycle

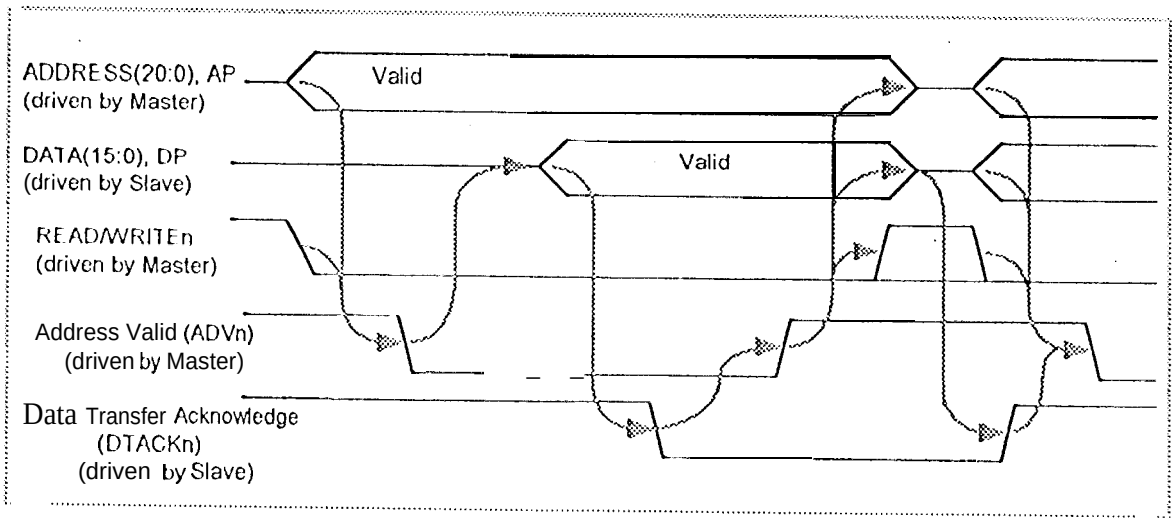

Figure 12: ISB Read Cycle

(6) Implementation Description

All four ASICs are implemented in Honeywell's RICMOS, 1,2 micron *process*, The ASICs are Class S parts produced on Honeywell's QML line. Their gate counts range from 18k to 25k gates. Some of their key performance parameters are:

KEY PERFORMANCE PARAMETERS	
Operating Voltage	4.5 to 5.5 Volts
Operating Temperature	-55 to -1 12s ^{O}C
Total Dose Radiation Hardness	>1 Mrad (Si)
Single Event Upset Rate	-"0.1 · upsets/year (galactic cosmic ray environment)
Dynamic Power Consumption	100 to 200 mW (maximum) per ASIC
Single Event latch-up	No latch-up @ LET= 120 MeV/mg/cm^2
Clock Frequency	12 MHz
Stuck-At Fault Coverage ""	>98.5%
Package type	256 pin leaded flat pack

The ASICs require very few external support chips in order to function. Those support chips that are required are described below:

HCD ASIC: The Critical Enable relays must be provided external to the ASIC. Also, the ASIC provides only digital outputs with 6 mA drive capability to control the Critical Enable relays. '] 'herefore, drive circuits for the relays arc also required. If the start-up PROM capability is used, then the PROM chips must be provided externally. An external decoder chip is also required to generate the chip selects for the PROMs. Depending on the application, differential line driver/receiver pairs are used on the interface to the uplink receiver.

RSDL ASIC: Two 8k by 8 (or 32k by 8) SRAM chips arc required. Depending on the application, differ ent ial line driver/rccciver pairs arc used on the inter-face to the downlink RF transmitter.

SSRU ASIC: Two 32k *by* 8 RAM chips are required. Depending on the application, differential line driver/receiver pairs are used on the interface to the Solid State Recorder.

XBA ASIC: *Onc* UTMC BCRTM chip, three 32k by 8 RAM *chips,* one 1553B transceiver, and two 1553B transformers arc required *each* for the RT and BC functions.

Since all of the ASIC outputs have 6 mA drivers, external drivers are typically not required, However, when driving a large capacitive load, external buffering may be rcqui[-eel,

(7) *Development Status*

Initially, a Field Programmable Gate Array (FPGA) version of each ASIC was developed and integrated into the subsystem. Testing of the FPGA designs has been successfully completed. The FPGA designs has been operating for more than 18 months.

After testing of the FPGA designs was completed, proc~f-of-design (} '01>) ASICs were built at 1 Ioneywell. The POD ASICs are identical to the ASICs that will be flown in space, except for a reduced level of screening. POD ASICs are currently available to external customers. Testing of the POD ASICs in the subsystem was completed in July, 1994. l'abdication of the flight ASICs is underway at Honeywell. Flight ASICs will be delivered to JPL in January, 1995, and will be available to external customers at that time.

CONCLUSION

The HCD, RSDL, SSRIU, and XBA ASICs, along with a host computer, can provide the user with a complete spacecraft Command and Data Subsystem. The uplink, downlink, and spacecraft intercommunication functions performed by the ASICs are generic functions required on every spacecraft. The fact that the ASICs adhere to widely used international and military standards make them particularly useful. The ASICs' high reliability (Class S) and radiation hardness should meet any user's needs. Functioning ASICs are currently operating in hardware and software testbeds at J]'I.. Proof-of-design ASICs arc currently available and flight ASICs will be available in January, 1995. The ASICs' ISB interface is a generic interface that the user can adapt to operate on a variety of buses. ASIC development is a high cost and high risk task that should be avoided when possible through the use ofofT-the-shelf ASICs.

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